Claims:

1. A bus system, comprising:

(a) a plurality of bus elements;

(b) a central unit having a plurality of bus inputs and an output, with the central unit coupling at least one of the inputs to the output;

(c) a first plurality of uni-directional point-to-point buses coupling the bus elements to the central unit bus inputs;

(d) a second plurality of uni-directional point-to-point buses coupling the output of the central unit to each of the bus elements; and

(e) arbitration logic granting the bus elements access through the central unit one at a time.

2. A system as recited in claim 1, wherein the system further includes a state device that is disposed at the output of the central unit.

3. A system as recited in claim 2, wherein the central unit comprises at least one OR gate, and the arbitration logic grants the bus elements access to associated first buses.

4. A system as recited in claim 2, wherein the central unit includes a multiplexer.

5. A system as recited in claim 4, wherein

the system further includes a state device at each input to the central unit, with the state devices also being connected to the arbitration logic.

6. A system as recited in claim 5, wherein the arbitration logic is part of the central unit.

7. A system as recited in claim 6, wherein the arbitration logic includes a scheduler and an arbiter.

~~8.~~ 10. A system as recited in claim 1, wherein the bus elements include a plurality of central processing units and a shared memory.

~~9.~~ 11. A system as recited in claim ~~8~~ 10, wherein the shared memory further comprises a plurality of memory modules with a single one of the first buses and a single one of the second buses being provided for coupling to the memory.

~~10.~~ 12. A system as recited in claim ~~8~~ 10, wherein the central unit further includes OR logic and the arbitration logic grants the bus elements access to associated first buses.

11. A system as recited in claim 10, wherein the OR logic, comprises:

a first OR gate which has as inputs the first buses from the plurality of central processing units, with the output of the first OR gate being coupled to the second bus for the shared memory; and

a second OR gate which has as a first input the output of the first OR gate and as a second input the first bus from the shared memory, with the output of the second OR gate being coupled to the second buses to the central processing unit.

14 ~~12~~. A system as recited in claim 13 ~~11~~, wherein the system further includes a state device that is connected to the output of the second OR gate, with the output of the state device being connected to the second buses leading to the central processing units.

15 ~~13~~. A system as recited in claim 14 ~~12~~, wherein the system further includes at least one driver between the output of the state device and the second buses leading to the central processing units.

16 ~~14~~. A system as recited in claim 10 ~~8~~, wherein ~~in~~ the central unit includes multiplexer circuitry ~~circuits~~ and arbitration logic for controlling the multiplexers.

17 ~~15~~. A system as recited in claim 16 ~~14~~, wherein the multiplexer circuitry ~~logic~~, comprises:

a first multiplexer which has as inputs a first bus

from each of the central processing units and providing an output coupled to the second bus from the central unit to the shared memory; and

a second multiplexer which has as a first input the output of the first multiplexer and as a second input the first bus from the shared memory to the central unit, with the output of the second multiplexer being connected to each of the second buses leading to the central processing units.

18 ~~16~~. A system as recited in claim 17 ~~15~~, wherein the system further includes a first state device at the output of the second multiplexer, with the output of the first state device being connected to the second buses leading to the central processing units.

19 ~~17~~. A system as recited in claim 18 ~~16~~, wherein the system further includes at least one driver between the output of the first state device and the second buses leading to the central processing units.

20 ~~18~~. A system as recited in claim 19 ~~17~~, wherein the central unit further includes a memory controller, with the memory controller providing at its output the second bus to the memory and having as an input the first bus from the memory, with the memory controller connecting the first bus to the second multiplexer and connecting the output of the first multiplexer to the

second bus.

Sub D3 19. The system as recited in claim 18, wherein the system further includes port select logic that connects each of the first buses from the central processing unit to the first multiplexer.

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~~20~~. The system as recited in claim ~~19~~, wherein for each input port coupled to one of the first buses, the port select logic includes:

an input state device;

a buffer having a plurality of locations, the input of the buffer coupled to the output of the input state device;

a port multiplexer having as inputs the outputs of the buffer locations and the output of the input state device; and

validity logic having as inputs the output of the state device and a control input from the arbitration logic for granting the port access to the bus system, with the validity logic providing an output to control the port multiplexer.

Sub D4 21. The system as recited in claim 20, wherein the arbitration logic includes an arbitrator and scheduling logic.

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~~22~~. The system as recited in claim ~~21~~,

wherein the outputs of the port multiplexers in the port logic for each of the central processing units is connected to the inputs of the first multiplexer, with the port select logic comprising logic responsive to the outputs of the port multiplexers and to an input from the arbitrator to control the first multiplexer such as to selectively couple one of its inputs to its output.

25 ~~23~~. The system as recited in claim 24 ~~22~~, wherein the scheduling logic includes logic to grant the input ports access on a round robin basis.

26 ~~24~~. A system as recited in claim 25 ~~23~~ 1, wherein ~~said~~ port select logic comprises:

a barrel shifter;

a first priority encoder having as inputs the outputs of the barrel shifter;

a schedule port ID multiplexer having as a first input the output of the priority decoder;

left shift one logic having an input coupled to the output of the first priority encoder and providing an output which is left shifted by one;

a next port multiplexer having as a first input the output of the left shift one logic;

a second state device coupled to the output of the next port multiplexer, the output of the second state device coupled back as a second input to next port multiplexer and as an input to the barrel shifter;

a third state device at the output of the schedule port ID multiplexer providing its output as a second input to the schedule port ID multiplexer, the output of the schedule port ID multiplexer also coupled to control the first multiplexer; and

port select logic for controlling the schedule port ID multiplexer to switch between the input of the priority encoder and the fed back input from the third state device.

25. The system as recited in claim 24, wherein each of the first buses includes at least one function code (FC) line indicative of the beginning and end of a transmission on the bus and the port select logic is responsive to the control line to switch the schedule port ID multiplexer to the next port.

~~26~~ 28. The system as recited in claim ~~25~~ 27, wherein the port select logic includes an old FC multiplexer having as inputs the FC lines from each of the ports, with the FC multiplexer being controlled by the output of the third state device; and

a port select generator having as one input the output of the old FC multiplexer and as a second input a scheduler grant input from the arbitrator.

~~27~~ 29. The system as recited in claim ~~28~~ 26, wherein at least some of the central processing units

include cache memory with each of the first buses including a "snoopy hit line" indicating that the addresses in a read command issued by another central processing unit are contained within its cache memory, with the port ~~schedule~~ select logic further comprising:

a second priority encoder having as inputs the "snoopy hit lines" from the buses;

an OR gate having as inputs said "snoopy hit lines", the output of the OR gate providing an input to the port select generator; and

the port select generator having as a further input a "snoopy hit shadow signal" indicating the period during which "snoopy hit signals" may occur, the output of the second priority encoder designating a "snoopy port" at which a "snoopy hit" has occurred and being coupled as a third input to the schedule port ID multiplexer, the port select generator, in response to receiving to the "snoopy hit signal" within the period of the "snoopy hit shadow" selects as the port to which access is to be granted, the "snoopy port" designated at the output of the priority encoder.

30. The system as recited in claim 29, wherein the central unit further includes at least one resource status unit including a memory map status unit indicating the status of modules in the shared memory, with the arbitrator including a resource check logic having as inputs the outputs from the resource status

units, the output of the first multiplexer and the output of the memory controller, the resource checker responsive thereto to provide outputs to the port logic and to the port select logic in the schedule logic and also to provide an output to the second multiplexer to select between resources, the resources including data from one of the central processing units at the output of the first multiplexer and memory data from the shared memory modules.

31. The system as recited in claim 30, wherein the resource check logic includes a command decoder receiving as an input the output from the first multiplexer; and

a command and resource check module having as one input the output of the command decoder and as additional inputs the outputs of the units indicating the status of modules of the shared memory; and

a timing circuit for generating the "snoopy hit shadow".

30. A system comprising:

a plurality of central processing units;

a shared memory;

a central unit including:

combining logic for accepting a plurality of inputs at least equal to the number of the central processing units plus memory and coupling at least one

of inputs to its output;

arbitration logic for controlling which of the inputs is provided at the output;

a memory controller providing a memory input to the combining logic and receiving a memory output from the combining logic;

a plurality of first uni-directional point-to-point buses, with one bus coupling each of the central processing units to an input of the combining logic;

a first uni-directional memory bus coupling the memory to the memory controller;

a plurality of second uni-directional point-to-point buses coupling the output of the combining logic to the central processing units; and

a second uni-directional memory bus coupling the output of the memory to the memory control logic.

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~~31~~. A system as recited in claim 33
~~30~~, wherein the combining logic comprises two stages of combining logic, a first stage of combining logic having the first buses from the central processing units as inputs and providing its output to the memory controller; and

a second stage of combining logic having as inputs the output of the first stage of combining logic and the output of the memory controller, with the output of the second stage of combining logic being provided to the second buses coupled to the plurality of central processing units.

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~~32~~. A system as recited in claim ~~31~~, wherein the first and second stages of combining logic comprise first and second multiplexers, and the arbitration logic comprises logic for controlling the multiplexers.

~~33~~. A method of implementing a high speed bus to which a plurality of bus elements are coupled comprising the steps of:

(a) coupling each of the bus elements to a central unit with a separate first uni-directional bus having a direction from the bus elements to the central unit;

(b) selecting one of the first bus inputs to the central unit to be an output; and

(c) coupling said output to each of the bus elements over a second uni-directional bus having a direction from the central unit to the bus elements.

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~~34~~. The method as recited in claim ~~33~~, wherein the bus elements include a plurality of central processing units and a shared memory.

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~~35~~. The method as recited in claim ~~34~~, wherein the selecting step further comprises selecting between the inputs on the first buses from the central processing ~~unit~~ units and the bus from the memory.

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~~36~~. The method as recited in claim ~~36~~,

wherein the central processing units output commands requesting access to the memory, each command followed by an address and/or data and/or additional commands and further including:

storing up to three words output by a central processing unit at the central unit;

arbitrating access to the bus at the output of the central unit, including granting access to one of the central processing unit inputs by providing the stored command to the output and on successive cycles providing additional words stored at the central unit on the output; and

when all stored words have been provided on the output on the next and subsequent cycles providing any input words from the central processing unit directly on the output whereby, by storing a number of words in the central unit, once the central processing unit is granted access to the bus, a continual flow of data will occur without any dead time.

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